U.S. DEPARTMENT OF COMMERCE PATENT & TRADEMARK OFFICE

B/O Form PTO 1390	Transmittal Letter to the United States Designated/Elected Office (DO/EO/US) Concerning a Filing Under 35 U.S.C. § 371	Attorney's Docket Number HITA.0099
		US Application Number (if known) 09/914429
International Application Number PCT/JP99/01035	International Filing Date 4 March 1999	Priority Date Claimed
Title of Invention SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD OF DESIGNING LOGIC INTEGRATED CIRCUIT		
Applicant(s) for DO/EO/US Masayuki SATO, Takayuki OSHIMA, Isao SHIMIZU and Hideaki TAKAHASHI		

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items under 35 U.S.C. § 371:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. § 371.

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. § 371.

3. ☒ This express request to begin national examination procedures *(35 U.S.C. § 371(f))* at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. § 371(b) and PCT Articles 22 and 39(1).

4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed *(35 U.S.C. § 371(c)(2))*
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).

6. ☐ A Verified Translation of the International Application into English *(35 U.S.C. § 371(c)(2))*.

7. ☐ Amendments to the claims of the International Application under PCT Article 19 *(35 U.S.C. § 371(c)(3))*
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 *(35 U.S.C. § 371(c)(3))*.

9. ☐ An oath or declaration of the inventor(s) *(35 U.S.C. § 371(c)(4)*.

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 *(35 U.S.C. § 371(c)(5))*.

Items 11 to 16 below concern other document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 C.F.R. §§ 1.97 and 1.98.

12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. §§ 3.28 and 3.31 is included.

13. ☒ A **FIRST** preliminary amendment.
    ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.

14. ☐ A substitute specification.

15. ☐ A change of power of attorney and/or address letter.

16. ☐ Other items or information:

Application Number (if known) 09/914429	International Application Number PCT/JP99/01035	Attorney's Docket Number HITA.0099	
		CALCULATIONS	PTO USE ONLY
17. ☒ The *following fees are submitted:* **Basic National Fee** *(37 C.F.R. § 1.492(a)(1)-(5))*			
☒ Search report has been prepared by the EPO or JPO $860.00			
☐ International Preliminary Examination Fee paid to USPTO *(37 C.F.R. § 1.482)* ... 690.00			
☐ No International Preliminary Examination Fee paid to USPTO *(37 C.F.R. § 1.482)* but International Search Fee paid to USPTO *(37 C.F.R. § 1.445(a)(2))* 710.00			
☐ Neither International Preliminary Examination Fee *(37 C.F.R. § 1.482)* nor International Search Fee *(37 C.F.R. § 1.445(a)(2))* paid to USPTO 1,000.00			
☐ International Preliminary Examination Fee paid to USPTO *(37 C.F.R. § 1.482)* and all claims satisfied provisions of PCT Article 33(2)-(4) 100.00			
	ENTER APPROPRIATE BASIC FEE AMOUNT	**$860.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date *(37 C.F.R. § 1.492(e))*.		**0.00**	
CLAIMS	**NUMBER FILED** / **NUMBER EXTRA** / **RATE**		
Total Claims	20 / 0 / x $18.00	**$0.00**	
Independent Claims	2 / 0 / x $80.00	**$0.00**	
Multiple dependant claims (*if applicable*)	2 / + $270.00	**$540.00**	
	TOTAL OF ABOVE CALCULATIONS	**$1,400.00**	
Reduction by ½ for filing by small entity, if applicable. Verified Small Entity Statements must also be filed. *(Note 37 C.F.R. §§ 1.9, 1.27, 1.28)*		**1,400.00**	
	SUBTOTAL	**$ 1,400.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☒ 30 months from the earliest claimed priority date *(37 C.F.R. § 1.492(f))*.		**$0.00**	
	TOTAL NATIONAL FEE	**1,400.00**	
Fee for recording the enclosed assignment *(37 C.F.R. § 1.21(h))*. The assignment must be accompanied by an appropriate cover sheet *(37 C.F.R. §§ 3.28, 3.31)*. **$40.00** per property		**$0.00**	
	TOTAL FEES ENCLOSED	**$ 1,400.00**	
Amount to be:		**Refunded:**	**$**
		Charged:	**$**

a. ☒ A check in the amount of **$1,400.00** to cover the national fees is enclosed.

b. ☐ Please charge my **Deposit Account Number 08-1480** in the amount of **$**_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to **Deposit Account Number 08-1480**. A duplicate copy of this sheet is enclosed.

Note.: Where an appropriate time limit under *37 C.F.R. § 1.94 or 1.495* has not been met, a petition to revive *(37 C.F.R. § 1.137(a) or (b))* must be filed and granted to restore the application to pending status.

Respectfully submitted,

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August 29, 2001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of	)
	)
SATO et al.	)
	)
Application Number: To be assigned	)
	)
Filed: Concurrently herewith	)
	)
For: SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD FOR DESIGNING LOGIC INTEGRATED CIRCUIT	)
	)

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Applicants have amended the claims in order to remove the multiple dependencies contained therein in accordance with standard U.S. practice, thereby reducing the basic filing fee. No new matter has been added to the application as a result of this amendment. Prior to an examination on the merits, please amend the above-identified application as follows:

IN THE CLAIMS:

Please substitute claims 3 and 4 currently on file with the following amended claims.

3. (Amended) A semiconductor integrated circuit according to claim 1, wherein the storing means are a volatile memory.

4. (Amended) A semiconductor integrated circuit according to claim 1, wherein the variable address converting means comprise: a memory array in which a plurality of memory cells are arranged in a matrix shape; an address decoder that selects the memory cells in the memory array based on an input address signal; reading means that amplify a signal read

from the memory array; and operating means that update the input address signal based on a control signal.

Please add the following new claims:

17. (Added) A semiconductor integrated circuit according to claim 2, wherein the storing means are a volatile memory.

18. (Added) A semiconductor integrated circuit according to claim 2, wherein the variable address converting means comprise: a memory array in which a plurality of memory cells are arranged in a matrix shape; an address decoder that selects the memory cells in the memory array based on an input address signal; reading means that amplify a signal read from the memory array; and operating means that update the input address signal based on a control signal.

19. (Added) A semiconductor integrated circuit according to claim 3, wherein the variable address converting means comprise: a memory array in which a plurality of memory cells are arranged in a matrix shape; an address decoder that selects the memory cells in the memory array based on an input address signal; reading means that amplify a signal read from the memory array; and operating means that update the input address signal based on a control signal.

20. (Added) A semiconductor integrated circuit according to claim 17, wherein the variable address converting means comprise: a memory array in which a plurality of memory cells are arranged in a matrix shape; an address decoder that selects the memory cells in the memory array based on an input address signal; reading means that amplify a signal read from the memory array; and operating means that update the input address signal based on a control signal.

REMARKS

Applicant has amended claim 3 and added claim 17, and amended claim 4 and added claims 18, 19 and 20. Applicants have amended the claims in order to remove the multiple dependencies contained therein in accordance with standard U.S. practice, thereby reducing the basic filing fee. No new matter has been added to the application as a result of this amendment.

In view of the above amendments and Applicants' comments stated herein, Applicants respectfully request an early and favorable action on the merits.

Respectfully submitted,

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August 29, 2001

Marked-up Version of Claims

CLAIMS:

1. A semiconductor integrated circuit, comprising:

storing means that enables reading and writing;

comparing means that compare write data supplied to the storing means with data read from the storing means; and

variable address converting means that convert an address signal supplied to the storing means based on a comparison result in the comparing means, wherein an input signal of a logic circuit having a desired logical function is input as the address signal to the storing means, and wherein the data is written to the storing means so that the read data of the storing means can be obtained as an expected output signal with respect to the input signal of the logic circuit.

2. A semiconductor integrated circuit according to claim 1, wherein a plurality of the storing means, a plurality of the comparing means, and a plurality of the variable address converting means are provided on a single semiconductor chip.

3. A semiconductor integrated circuit according to claim 1 ~~or 2~~, wherein the storing means are a volatile memory.

4. A semiconductor integrated circuit according to claim 1, ~~2, or 3,~~ wherein the variable address converting means comprise: a memory array in which a plurality of memory cells

Application for
UNITED STATES LETTERS PATENT

of

MASAYUKI SATO

TAKAYUKI OSHIMA

ISAO SHIMIZU

and

HIDEAKI TAKAHASHI

for

SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD FOR DESIGNING LOGIC INTEGRATED CIRCUIT

14/pats

SPECIFICATION

TITLE OF THE INVENTION

SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD FOR DESIGNING LOGIC INTEGRATED CIRCUIT

TECHNICAL FIELD

The present invention relates to the design of a semiconductor integrated circuit, and, more particularly, to an effective technique used for a construction system of a logic integrated circuit.

BACKGROUND ART

In recent years, the development, that is, design through its trial manufacture of a logic integrated circuit has been being performed in accordance with the procedure shown in Fig. 15. That is, in the development of the logic integrated circuit, as shown in Fig. 15, first, the functional design of the logic integrated circuit to be realized is performed. Next, a designed function is described in language, such as HDL (hardware description language). Further, the design data (HDL descriptive statement) described in this HDL is stored as a data file in a storage device, such as a hard disc. Besides, regarding an HDL description, a support tool (program) that automatically creates the HDL descriptive statement from a state transition drawing and a flowchart is offered by EDA (engineering design

automation) vendors.

Next, the design data described in the HDL is verified with a verification program called a test vector as to whether an operation is appropriate. If a defect is detected by verification, the HDL descriptive statement is modified.

Subsequently, the design data described in the HDL is converted to the design data of a logic gate level with a program called a logic synthesis tool. Such logic synthesis tool is also offered by multiple EDA vendors. The design data of a generated logic gate level is re-verified with the test vector. The ratio of failure detection at this time is 95% or more, for example. When a defect is found by the verification, the design data of the logic gate level is modified.

In the next place, based on the design data of the logic gate level, layout data of an element level is generated with a program called an automatic layout tool. Such automatic layout tool is also offered by multiple EDA vendors. An actual load simulation is run on the generated layout data according to the test vector including a wiring time delay or the like, and inappropriate places are modified and optimized. Subsequently, mask pattern data is generated by artwork based on the generated layout data and a mask is created based on this data.

Subsequently, a logic integrated circuit is formed on a semiconductor wafer according to the pre-process. The wafer is

cut into each chip and sealed with a sealing material, such as resin and assembled into a package. However, in such design and manufacturing systems as above, since the design data in several stages is created via many design processes until the logic integrated circuit is completed as the final logic integrated circuit device, the data increases in quantity. Further, since a system on chip in which the entirety of a system is constructed on a single semiconductor chip is constructed by using various function circuit blocks, turn around time of the verification and modification of the design data is increased, thereby raising a great problem in design.

Further, in the conventional design technique, as an element is scaled down, the number of masks used for manufacturing a single semiconductor integrated circuit (also called IC) increases, and an expensive manufacturing apparatus is required for microfabrication, thereby increasing design and manufacturing costs and decreasing a yield.

Moreover, in the conventional design technique, since an individual mask must be fabricated for each product, the period required for the development of a new product is prolonged. Further, in the microfabrication of deep submicron (less than 0.1 μm) that will be estimated to be realized in future, an SOR (synchrotron) apparatus is required. Accordingly, in a single semiconductor device manufacturer, the investment becomes difficult and an amount of investment for the microfabiracation

is approaching to the limit.

An object of the present invention is to provide a design technique of a logic integrated circuit that can greatly reduce a design man-hour and a development period.

Another object of the present invention is to provide a logic integrated circuit of which the function can easily be modified as needed.

A further object of the present invention is to provide a logic integrated circuit that can construct a normal function by substituting for a defect even if there is the defect in some elements of a finished product.

The aforementioned and other objects of the present invention and its new characteristics will be evident from a description of this specification and appended drawings.

DISCLOSURE OF THE INVENTION

An outline of the typical invention among the inventions disclosed in this application is described below.

That is, a logic integrated circuit having a desired logical function is constructed by decoding design data of a function level described in language, such as HDL in a control circuit using a self-construction circuit formed into a semiconductor integrated circuit that can construct optional logic and assigning a signal that decides the logical configuration of the self-construction circuit from the control

circuit to the self-construction circuit.

The self-construction circuit includes a memory circuit that enables reading and writing, a comparator that compares write data supplied to the memory circuit and data read from the memory circuit, and a variable address conversion circuit that converts an address signal supplied to the memory circuit based on a comparison result in the comparator, and data is written to the memory circuit so that an input signal of a logic circuit having a desired logical function is used as the address signal to the memory circuit and the read data of this memory circuit will become an expected output signal against the input signal of the logic circuit.

HDL has a similar structure to that of existing general program language, and software that performs logic synthesis based on design data of a function level described in the HDL, that is, the HDL descriptive language and software that converts the logically synthesized design data to design data of a logic gate level have already been developed, Accordingly, a control circuit for generating a signal that decides the logical configuration of the self-construction circuit based on the design data of the function level can be fully realized using the current technique.

According to the design technique, in the development of a logic integrated circuit, since only a HDL descriptive statement may be created and the logic synthesis based on the

HDL descriptive statement and its verification and the conversion of logically synthesized design data to design data of a logic gate level and its verification are not required, a designing turn around time and a development period can greatly be reduced. Further, since a support tool (program) that automatically creates the HDL descriptive statement from a state transition drawing and a flowchart is offered by EDA vendors, the HDL descriptive statement is also comparatively easily created.

Further, since the present invention constructs logic using a self-construction circuit having a memory circuit that enables reading and writing, a logical function can be changed by rewriting the memory circuit and a logic integrated circuit of which the function change is easy can be realized as needed.

Moreover, since the self-construction circuit has a comparator that compares the write data supplied to the memory circuit and the data read from the memory circuit and a variable address conversion circuit, a conversion address of the variable address conversion circuit can be constructed performing the self-verification of logic to be constructed. Further, if the memory circuit contains a defective part, the logic can be constructed avoiding the defective part and using only a normal area. Accordingly, even if there is a defect in some elements, a normal function can be constructed by automatically avoiding it.

Besides, the control circuit that decodes design data of a function level may also be constructed as a semiconductor integrated circuit that differs from the self-construction circuit, or may also be constructed on a single semiconductor chip by being integrated with the self-construction circuit. When the control circuit that decodes the design data of the function level and the self-construction circuit are integrated, even a storage that stores the design data of the function level ought to be integrated.

Consequently, a self-constructive logic integrated circuit having a desired logical function by its own judgment and processing can fully be realized by merely storing a design statement described at a function level in the storage. Further, a part of the area of the memory circuit that constructs the self-construction circuit can also be used as a storage area in which the design data of the function level is stored. For example, the design data of the function level described in the HDL can sufficiently be stored in the memory circuit formed in a semiconductor integrated circuit, since the data amount is about one tenth, compared with the design data of a logic gate level.

Further, if a constructing logical function contains not only a combinational circuit but also a sequential circuit, as the self-construction circuit, in addition to the memory circuit that enables reading and writing described above, a comparator

that compares the write data supplied to the memory circuit and the data read from the memory circuit, and an address conversion circuit that converts an address signal supplied to the memory circuit based on the comparison result in the comparator, a data storage circuit that holds the data from the memory circuit and a switch matrix circuit that switches the data held in the data storage circuit to the address signal input to the address conversion circuit may be provided. Accordingly, the sequential circuit that contains a latch circuit, such as a flip-flop can be constructed.

As the language that describes the design data of the function level, for example, the HDL can be used. As the memory circuit that enables reading and writing contained in the self-construction circuit, a volatile memory, such as a DRAM (dynamic random access memory) or SRAM (static random access memory), is desirable. However, an electrically write-enable and erasable nonvolatile memory device (EEPROM: electrically erasable programmable read-only memory) may be used. By using the volatile memory, a surplus voltage step-up circuit needs not to be provided and low voltage drive is enabled. Further, if the DRAM is used instead of the SRAM, an occupied space is reduced with respect to the same storage capacity and a chip size can be reduced. On the other hand, if the SRAM is used instead of the DRAM, there is an advantage that the refresh operation peculiar to the DRAM is not required.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a flowchart showing a development procedure of a logic integrated circuit to which the present invention applies;

Fig. 2 is a block diagram showing a first embodiment of a self-construction circuit that enables a design technique according to the present invention;

Fig. 3 is a block diagram showing a specific example of a variable address conversion circuit contained in the self-construction circuit of the first embodiment;

Fig. 4 is a logical configuration drawing showing a specific example of a comparator contained in the self-construction circuit of the first embodiment;

Fig. 5 is a flowchart showing a method for changing a conversion address in the self-construction circuit of the first embodiment;

Fig. 6 is an explanatory drawing showing an example of a logic gate circuit constructed by the self-construction circuit of the first embodiment and its HDL descriptive statement;

Fig. 7 is a block diagram showing an example of a system that constructs a logic circuit of a desired logical function in accordance with the HDL descriptive statement using the self-construction circuit of the first embodiment;

Fig. 8 is a block diagram showing a second embodiment of the self-construction circuit that enables the design technique according to the present invention;

Fig. 9 is a circuit block diagram showing a specific example of a variable switch circuit contained in the self-construction circuit of the second embodiment;

Fig. 10 is a logical configuration drawing showing a specific example of a data storage circuit contained in the self-construction circuit of the second embodiment;

Fig. 11 is an explanatory drawing showing a flip-flop circuit as an example of the logic circuit constructed by the self-construction circuit of the second embodiment and its HDL descriptive statement;

Fig. 12 is a flowchart showing an outline of the processing procedure in a controller when a desired logic circuit is constructed using the self-construction circuit of the first or second embodiment;

Fig. 13 is a block diagram showing a third embodiment of the self-construction circuit that enables the design technique according to the present invention;

Fig. 14 is a block diagram showing a fourth embodiment of the self-construction circuit that enables the design technique according to the present invention; and

Fig. 15 is a flowchart showing a development procedure of a conventional logic integrated circuit.

BEST MODE FOR CARRYING OUT THE INVENTION

Ideal embodiments of the present invention are described below with reference to the drawings.

Fig. 1 is a flowchart showing a development procedure of a logic integrated circuit to which the present invention applies.

First, the functional design of the logic integrated circuit to be realized is performed (step S1). Next, the designed function is described (step S2) in language, such as HDL and stored in a storage device, such as a hard disc as a data file (step S3). Besides, regarding an HDL descriptive statement, as described previously, since a support tool that automatically creates the HDL descriptive statement from a state transition drawing and a flowchart is offered by EDA venders, the statement ought to be created using such tool.

Next, the design data described in HDL is verified as to whether an operation is appropriate with a verification program called a test vector (step S4). If a defect is detected by the verification, the design data described in the HDL is modified.

Subsequently, the logical function described in the HDL is constructed using the self-construction circuit formed as a semiconductor integrated circuit (step S5). Since a logic integrated circuit having a desired function can be obtained according to the procedure, a development period can greatly

be reduced.

Fig. 2 shows a block diagram of a first embodiment of the self-construction circuit that enables the design technique according to the present invention in accordance with the flowchart of Fig.1. Besides, each circuit block shown in Fig. 2 is formed on a single semiconductor chip, such as a single crystal silicon, by known semiconductor manufacturing technique.

In Fig. 2, 10 is a read- and write-enable memory circuit having almost the same configuration as a known general-purpose DRAM (dynamic random access memory) or SRAM (static random access memory).

That is, the memory circuit 10 is provided with a memory array 11 in which multiple memory cells are arranged in a matrix shape, multiple word lines and multiple data lines are arranged in a matrix shape, the memory cells on the same line are connected to the corresponding word lines respectively, and the memory cells on the same column are connected to the corresponding data lines respectively, an address decoder 12 that decodes a supplied address signal and sets the corresponding single word line of the memory array 11 to a selected level, a sense amplifier circuit 13 that amplifies the potential read from the memory cell connected to a selected word line to a data line, and a write and read control circuit 14 that controls operation timing, such as the sense amplifier circuit 13 based on a chip selection signal

CE and a write control signal WE.

The self-construction circuit of this embodiment, in addition to the memory circuit 10, comprises: an input/output & comparator 20 that fetches write data input from the external of a chip, transfers it to the sense amplifier circuit 13, outputs the data read from the memory circuit 10 to the external of the chip, and compares the read data with the data input from the external of the chip; and a variable address conversion circuit 30 that converts an address signal input from the external of the chip in accordance with a comparison result in the input/output & comparator 20 and supplies it to the address decoder 12.

Reference numeral 41 is an address input terminal to which the address signal from the external of the chip is input and 42 is a data input/output terminal that outputs the read data from the memory circuit to the external and inputs the write data from the external.

Fig. 3 is a block diagram showing a specific example of the variable address conversion circuit 30 contained in the self-construction circuit of the embodiment of Fig. 2. This variable address conversion circuit 30 has almost the same circuit configuration as the memory circuit 10 of Fig. 2.

That is, the variable address conversion circuit 30 is provided with a memory array 31 in which multiple memory cells are arranged in a matrix shape, multiple word lines and multiple

data lines are in a matrix shape, the memory cells on the same line are connected to the corresponding word lines respectively, and the memory cells on the same column are connected to the corresponding data lines respectively, an address decoder 32 that decodes the address signal supplied to the input terminal 41 from the external and sets the corresponding single word line of the memory array 31 to a selected level, a sense amplifier circuit 33 that amplifies the potential read from the memory cell connected to the selected word line to the data line, and a write control circuit 34 that controls the operation timing of the sense amplifier circuit 33 based on a comparison result signal CM from the input/output & comparator 20.

Although not shown, the address decoder 32 includes an incrementor that increments a decoder and an address to be decoded based on the comparison result signal CM or an arithmetic unit. Further, an incremented value is stored in the memory 31 and the storage capacity of 31 may be also reduced.

Fig. 4 shows a specific example of the input/output & comparator 20 contained in the self-construction circuit of the first embodiment.

As shown in Fig. 4, the input/output & comparator 20 comprises: a switching means 21 that is controlled with a comparison instruction signal CC supplied from the write and read control circuit 14 provided between a signal line 51 connected to the output terminal of the sense amplifier 13 and

a signal line 52 connected to the data input/output terminal 42; a NAND gate circuit 22 that uses a read signal from the sense amplifier circuit 33 and the comparison instruction signal CC supplied from the write and read control circuit 14 as input signals; an exclusive OR gate circuit 23 that uses an output signal of the NAND gate circuit 22 and a signal input from the data input/output terminal 42 as inputs; and an OR gate circuit 24 that uses output signals of the multiple exclusive OR gate circuits 23 as inputs.

That is, a comparator having the switching unit 23, the NAND gate circuit 22, and the exclusive OR gate circuit 23 is provided in each data input/output terminal 42. The output signal of the exclusive OR gate circuit 23 in each comparator is input to the OR gate circuit 24 and the output signal of the OR gate circuit 24 is supplied to the variable address circuit 30 as the comparison result signal CM. Besides, although not shown, an input buffer and an output buffer connected in common to the data input/output terminal 42 may be also provided at the signal line 52 side.

Next, the method for changing a conversion address in the self-construction circuit of the embodiment is described using the flowchart shown in Fig. 5. Besides, before the flowchart shown in Fig. 5 is started, in the address conversion circuit 30, an address that corresponds to each number of the memory circuit 10 is stored in each address of the memory array 31 by

initial set processing or the like.

When an address signal is input from the address input terminal 41 from the external, the address decoder 32 of the variable address circuit 30 decodes the address signal. The corresponding word line of the memory array 31 is set at a selected level and the previously stored address data is output, that is, address-converted (step S11). The read address data is amplified by the sense amplifier 33 and supplied to the address decoder 12 of the memory circuit 10. The address decoder 12 decodes the supplied address and sets the corresponding word line at the selected level, and then, writes the data input from the external to the memory cell via the input/output & comparator (step S12).

Next, the write data is read from the memory array 11 (step S13). The read data is amplified by the sense amplifier 13 and supplied to the input/output & comparator 20. At this time, the write data that is input when the data is written is input to the data input/output terminal 41. Accordingly, the input/output & comparator 20 compares the data read from the memory array 11 with the write data input to the data input/output terminal 41 and outputs the comparison result signal CM indicating a match or mismatch to the write control circuit 34 of the variable address conversion circuit 30.

Subsequently, the write control circuit 34 decides whether writing is normally performed or not referring to the comparison

result signal CM (step S14). Hereupon, when the write control circuit 34 decides that the writing is not successful, a signal is sent to the address decoder 32 and an internal incrementor is operated, and then an input address signal is incremented (step S15). Hereupon, this incremented address is supplied to the address decoder 12 and decoded, and the next word line of the memory array 11 is set at a selected level. Then processing returns to the step S12 and the data input from the external is written to a selected memory cell connected to the word line via the input/output & comparator 20.

Next, the write data is re-read from the memory array 11 and compared by the input/output & comparator 20 with the data input to the data input/output terminal 42 from the outside. Subsequently, when both data match, the write control circuit 34 outputs a write end signal WF to the external and the data write operation for one address terminates (step S16). When an external control circuit receives the write end signal WF, the next address signal is generated and input to the address input terminal 41. In response to this, the write control flow of Fig. 5 is restarted from the step S1 and the next address write processing is executed.

As described above, in this embodiment, the write data is read after the data is written and whether the data is normally written is decided. If an error is detected in the decision, an address is updated and the data is written to the next address

position. Accordingly, even if there is a defect in the memory array 11, the address is automatically skipped and the data is written to the next address. Thus, in the self-construction circuit of this embodiment, there is an advantage that all the memory cells of the memory array 11 need not to be normal, and previous test whether there is a detective bit in the memory array 11 is not needed.

Besides, in the above embodiment, the case where writing is performed by deciding whether there is a defect in the memory array 11 or not is described. The output signal line of the sense amplifier 33 in the variable address conversion circuit 30 of Fig. 2 is constructed so as to be supplied to the input/output & comparator 20 as well as the address decoder 12 of the memory circuit 10. Subsequently, the normality or abnormality of the write data to the memory array 31 is decided in the same manner as described above and an address is skipped in case of the abnormality. Accordingly, even regarding the memory array 31, all the memory cells need not to be normal, and previous test that there is a defective bit in the memory array is not needed.

Fig. 6 shows an example of the logic gate circuit constructed by the self-construction circuit of the first embodiment and the HDL descriptive statement. Further, Fig. 7 shows an example of a system that constructs a logic circuit having a desired logical function in accordance the HDL descriptive statement using the self-construction circuit of

the first embodiment.

In Fig. 7, reference numeral 100 is the self-construction circuit of the embodiment and 200 is a storage unit (file) that stores the design data described in the HDL, as described in Fig. 6. Reference numeral 300 is a controller that forms a signal for decoding the HDL descriptive statement stored in the file and constructing the corresponding logical function in the self-construction circuit 100. This controller 300 can be constructed using a general-purpose microcomputer, for example.

Next, a method of a specific logical configuration is described quoting the NAND gate circuit of Fig. 6 as an example. First, the controller 300 decodes the HDL descriptive statement and recognizes that a configuration object is a NAND gate circuit. For example, combinations "0, 0", "1, 0", "0, 1", and "1, 1" of input signals In0 and In1 listed in the truth table of the following Table 1 are generated as the address signals supplied to the self-construction circuit 100.

Subsequently, these generated address signals are assigned to the address input terminal 41 (refer to Fig. 2) of the self-construction circuit 100. Simultaneously, the controller 300 generates the data that corresponds to the output Out0 of the truth table as the write data that corresponds to each of the addresses and the write data is assigned to the data input/output terminal 42 in parallel to the input of the address signal with time.

Hereupon, in the self-construction circuit 100, the data is written to the memory circuit 10 in accordance with the procedure described using the flowchart of Fig. 5. Accordingly, after writing terminates, when the input signals In0 and In1 of the NAND gate are input to the predetermined address input terminal circuit 41 of the self-construction circuit 100, the corresponding data stored in the memory circuit is read and the signal that corresponds to the output Out0 of the NAND gate circuit is output from the predetermined terminal of the data input/output terminal 42. When the self-construction circuit of the embodiment of Fig. 2 is used in this manner, a desired logical function will be realized by writing data to the memory circuit 10 in accordance with the HDL descriptive statement.

Table 1

In0(In2)	In1(In3)	Out0(Out1)
0	0	1
1	0	1
0	1	1
1	1	0

When only a 2-input NAND gate circuit as described above is constructed using the self-construction circuit of Fig. 2, the input address signal may be two bits. Accordingly, the address decoder 32 shown in Fig. 3 has the configuration in which addresses are split every two bits, for example, and the single word line of the memory array 31 should be able to be selected

using the two bits.

Accordingly, multiple logic gate circuits can be realized by a single self-construction circuit. Further, to provide the same address configuration as the conventional memory and realize the multiple logic gate circuits with a single memory array, an address bit other than the input bit needs to be compensated, but an address needs not to be compensated if the address is split as described above. However, the memory array of which the address is not split can also be used by assigning a number to each a logic gate circuit that constructs logic to be realized and specifying the number combined with the input bit as a compensation address for the address of the logic gate to be aimed at.

Fig. 8 is a block diagram showing a second embodiment of the self-construction circuit that enables the design technique according to the present invention.

In this embodiment, a data storage 60 and a switch matrix 70 as a variable switching circuit are added to the self-construction circuit of the first embodiment shown in Fig. 2. The data storage 60 holds the data read from the memory circuit 10 or the previous input data input from the data input/output terminal 42 and is provided between the input/output & comparator 20 and the data input/output terminal 42. The switch matrix 70 is a circuit for supplying the data held in the data storage 60 to the variable address conversion circuit 30 instead of an

input address signal and provided between the address input terminal 41 and the variable address conversion circuit 30.

Besides, the data storage 60, the memory circuit 10 other than the switch matrix 70, the input/output & comparator 20, and the variable address conversion circuit 30 have quite the same configuration as the first embodiment.

Fig. 9 is a circuit block diagram showing a specific example of the switch matrix 70 contained in the self-construction circuit (Fig. 8) of the second embodiment.

The switch matrix 70, as shown in Fig. 9 (A), is arranged in a grid shape so that multiple signal lines 71 to which the address signal input to the address input terminal 41 is issued and a signal line 72 to which the output signal of the data storage 60 is issued are mutually intersected and a changeover switch circuit 73 is arranged in each intersection of the signal lines 71 and 72. Simultaneously, a RAM 74 that stores the control information of each changeover switch circuit 73 is provided.

The changeover switch circuit 73, as shown in Fig. 9 (B), is provided with switch elements SW1 and SW2 having a pair of MOSFETs that complementarily enter the on and off states in order to select the address signal input from the address input terminal 41 or the output signal of the data storage 60 and output it. Further, the gate terminal of the respective switch elements SW1 and SW2 is constructed so as to be controlled in accordance with the control information stored in the RAM 74.

However, instead of providing the RAM 74, as shown in Fig. 9 (c), the configuration in which the same static memory cell MC as the SRAM cell and a changeover switch CSW are provided in each intersection of the signal line 71 and the signal line 72 respectively ought to be also acceptable.

Fig. 10 is a logical configuration drawing showing a specific example of the data storage circuit 60 contained in the self-construction circuit (Fig. 8) of the second embodiment.

The data storage circuit 60, as shown in Fig. 10, is provided with flip-flops FF1, FF2, ...FFn provided corresponding to two data lines each of the memory array 11 of the memory circuit 10 and AND gates G1, G2, ... Gn for forming a latch clock of each flip-flop.

Subsequently, for each flip-flop FFi, the one signal (di) of a paired data line is input to a data input terminal D. Further, the other signal (Ai) of the paired data line is input to an AND gate Gi together with a system clock signal CLK. Subsequently, the output signal of this AND gate Gi is input to a clock terminal ck of the corresponding flip-flop FFi and the input signal to the data terminal D is fetched in the flip-flop FFi synchronizing with the trailing or leading edge of the signal to the clock terminal ck.

In the circuit of Fig. 10, when the signal Ai is set at the low level, the output of the AND gate Gi is fixed to the low level. Accordingly, the corresponding flip-flop FFi will

not perform any latch operation even if the system clock CLK varies. That is, in this embodiment, the signal Ai is used as a signal (hereinafter referred to as active bit) that controls whether to fetch data for the flip-flop FFi or not.

Since the self-construction circuit of the embodiment of Fig. 2 described previously can construct a combinational circuit, but cannot construct a sequential circuit because an output state (output data) is uniquely decided according to an input state (input address). On the contrary, the self-construction circuit of Fig. 8 selectively holds the data read from the memory circuit 10 in accordance with a certain input state by using the data storage 60 having the operation characteristics and can control the following input state according to the preceding output data by supplying this data to the variable address conversion circuit 30 via the switch matrix 70. That is, accordingly, the sequential circuit can be constructed.

Fig. 11 shows an example of a flip-flop circuit as an example of the logic circuit constructed by the self-construction circuit of the second embodiment shown in Fig. 8 and the HDL descriptive statement. The flip-flop circuit of Fig. 11 connects each output terminal of two NAND gate circuits G11 and G12 to the one input terminal of the other NAND gate circuit.

The truth table in which the output signal states that correspond to the input signals of the two NAND gate circuits

G11 and G12 for constructing this flip-flop circuit are indicated is shown in the following Table 2. In table 2, A1 or A2 is the active bit stored corresponding to the input of the memory circuit 10. Only when this active bit is "1", the output value of the flip-flop indicates that the truth value data of the corresponding NAND gate is output.

Table 2

	In0	In1	In2	In3	Out0		Out1	
					d1	A1	d2	A2
a	0	0	0	0	1	1	1	1
b	1	0	0	0	1	1	0	0
c	0	1	0	0	1	1	0	0
d	1	1	0	0	0	1	0	0
e	0	0	1	0	0	0	1	1
f	1	0	1	0	0	0	0	0
g	0	1	1	0	0	0	0	0
h	1	1	1	0	0	0	0	0
i	0	0	0	1	0	0	1	1
j	1	0	0	1	0	0	0	0
k	0	1	0	1	0	0	0	0
l	1	1	0	1	0	0	0	0
m	0	0	1	1	0	0	0	1
n	1	0	1	1	0	0	0	0
o	0	1	1	1	0	0	0	0
p	1	1	1	1	0	0	0	0

When the flip-flop circuit as shown in Fig. 11 is constructed using the self-construction circuit of Fig. 8, first, four input signals In0, In1, In2, and In3 are input from the address input terminal 41 to the variable address conversion circuit 30 via the switch matrix 70, and the output data items d1, A1, d2, and A2 of the second truth table of Table 2 that

correspond to the combinations of their input signals are input from the data input/output terminal 42. Accordingly, the output data items d1, A1, d2, and A2 of the truth table are written to the predetermined address of the memory array 11 of the memory circuit 10 using the input signals In0, In1, In2, and In3 as addresses. This embodiment is identical with the first embodiment in that the data is read after it is written and whether the data is normally written or not is decided, and when a write error occurs, the data is written to another address by changing the address.

Next, to set a feedback loop of a flip-flop circuit to be constructed, the state of the predetermined flip-flop (for example, FF1 or FF2) of the data storage 60 is set. Specifically, first, the input signals In2 and In3 are fixed to "0" respectively, and with a NAND gate circuit G11 aimed at, the input signals In0 and In1 are set to "0, 0", "1, 0", "0, 1", or "1, 1" in accordance with the data held in the flip-flop FF1 and input from the address input terminal 41.

Subsequently, as shown in the columns a, b, c, and d of Table 2 respectively, when the input signals In2 and In3 are fixed to "0" together, "1" is read as the active bit A1 that corresponds to the NAND circuit G1. Accordingly, the clock CLK is supplied to the flip-flop FF1 via the AND gate G1 of the data storage 60. As a result, in accordance with the combinations of the input signals In0 and In1 at that time, the data d1 of

"1" or "0" is fetched for the flip-flop FF1. That is, the state of the flip-flop FF1 is set.

Next, the input signals In0 and In1 are fixed to "0" respectively, and with the NAND gate circuit G11 aimed at, the input signals In2 and In3 are set to "0, 0", "1, 0", "0, 1", or "1, 1" in accordance with the data held in the flip-flop FF2 and input from the address input terminal 41.

Subsequently, as shown in the columns a, e, i, and m of Table 2 respectively, when the input signals In0 and In1 are set to "0" together, "1" is read as the active bit A2 that corresponds to the NAND gate circuit G2. Accordingly, the clock CLK is supplied to the flip-flop FF2 via the AND gate G2 of the data storage 60. As a result, the data d2 of "0" or "0" is fetched for the flip-flop FF2 in accordance with the combinations of the input signals In2 and In3 at that time. That is, the state of the flip-flop FF2 is set.

Besides, since the flip-flop having two NAND gates shown in Fig. 11 feeds back each output signal to the one input terminal of the other NAND gate, neither the output Out0 nor Out1 can be set to "0" at the same time. Accordingly, when the states of the flip-flop FF1 and FF2 of the data storage 60 are set, it needs to be noted that their holding states are not set to 0 together.

As described above, after the flip-flops FF1 and FF2 are set to a desired state, the storage data of the memory cell that

switches CSW31 and the CSW22 enclosed by a dotted line in Fig. 9 (A) in the control information RAM 74 of the switch matrix circuit 70 is rewritten and their switches are switched into the output terminal side of the data storage 60 from the side of the address input address input terminal 41. Accordingly, the input signals of the flip-flop of Fig. 11 are not allowed for their input, and the outputs Out0 and Out1 of the NAND gates G11 and G12 are supplied to the next stage variable address conversion circuit as the input signal (address) instead. That is, accordingly, a feedback loop for a flip-flop will be constructed.

Besides, the system that constructs a logic circuit having a desired logical function using the self-construction circuit of the second embodiment of Fig. 2 of Fig. 8 in accordance with the HDL descriptive statement may be identical with the system shown in Fig. 7 that constructs logic using the self-construction circuit of the first embodiment shown in Fig. 2. That is, the controller 300 constructed separately from the self-construction circuit decodes the HDL descriptive statement read from the file in which the design data described in the HDL is stored and forms and outputs a signal for constructing the corresponding logical function in the self-construction circuit 100.

The procedure of logically constructing the flip-flop circuit of such configuration as shown in Fig. 11 is described

using the self-construction circuit of the second embodiment of Fig. 8 according to the HDL descriptive statement based on the system of Fig. 7. First, the controller 300 decodes the HDL descriptive statement and recognizes that a configuration object is a flip-flop circuit. For example, as the address signals supplied to the self-construction circuit 100, the combinations "0, 0, 0, 0", "1, 0, 0, 0", "0, 1, 0, 0" ..... and "1, 1, 1, 1" of the input signals In0, In1, and In3 shown in the truth table of the following Table 2 are generated.

Then these generated address signals are assigned to the address input terminal 41 of the self-construction circuit 100. Simultaneously, the controller 300 generates the data that corresponds to the outputs D1 and d2 of the truth table and the corresponding active bit data items A1 and A2 as the write data that corresponds to each of the addresses and assigns them to the data input/output terminal 42 in parallel to the input of the address signal to the self-construction circuit 100 with time.

Subsequently, in the self-construction circuit 100, the data is written to the memory circuit 10 in accordance with the procedure described using the flowchart of Fig. 5. Accordingly, when the input signals In0 to In3 of the flip-flop circuit are input to the predetermined address input terminal 41 of the self-construction circuit 100 after writing terminates, the corresponding data items (output data bits d1 and d2 and active

bits A1 and A2) stored in the memory circuit are read. Subsequently, first, the output data that corresponds to the fact that the active bits A1 and A2 are "1" is fetched for the flip-flop FFi shown in Fig. 10. This is supplied to the variable address conversion circuit 30 via the switch matrix 70.

Accordingly, the next data is read from the memory circuit 10 in accordance with the previously read data and the signal that corresponds to the outputs Out0 and Out1 of the flip-flop circuit is output from the predetermined terminal of the data input/output terminal 42. When the self-construction circuit according to the embodiment of Fig. 8 is used in this manner, flip-flop logic can be constructed by writing the data to the memory circuit 10 in accordance with the HDL descriptive statement and a desired logical function including a sequential circuit is realized.

Fig. 12 shows an outline of the control procedure of the controller 300 that constructs the desired logic circuit. The controller 300, first, decodes the HDL descriptive statement (step S21) and extracts a combinational circuit and a sequential circuit that construct a logic circuit according to the HDL descriptive statement (step S22). Subsequently, a truth table, that is, truth value data regarding the extracted combinational circuit or the sequential circuit is generated (step S23). The data is written the memory circuit 10 of the self-construction circuit 100 and the variable address conversion circuit 30 is

set up (step S24).

Further, when the controller 300 decodes the HDL descriptive statement and decides that the extracted logic circuit is the sequential circuit, the circuit connection information of the sequential circuit to be aimed at is extracted (step S25). Subsequently, the control information stored in the control information RAM 74 of the switch matrix circuit 70 is generated and written (step S26).

Fig. 13 shows a third embodiment that enables the design technique according to the present invention.

In this embodiment, the multiple self-construction circuits 100 as shown in Fig. 8 are arranged on a single semiconductor chip in a matrix shape and a vertical wiring area 110 and a vertical wiring area 120 are provided between the respective self-construction circuits. A switch matrix circuit 130 is provided that can selectively couple a signal line in the intersection between the horizontal wiring area 110 and the vertical wiring area 120. Further, a switch matrix circuit 140 for selectively coupling the address input terminal of each self-construction circuit 100 with the signal line of the vertical wiring area 120 and a switch matrix circuit 150 for selectively coupling the data input/output terminal with the signal line of the vertical wiring area 110 are provided.

By providing the multiple self-construction circuits 100 on a single semiconductor chip, a larger scale logic integrated

circuit having a desired logical function can be constructed in accordance with the HDL descriptive statement.

Fig. 14 shows a fourth embodiment of the self-construction circuit that enables the design technique according to the present invention.

In this embodiment, a self-construction circuit 100' shown in Figs. 2, 8, and 13, an HDL storage 200' that stores the design data described in the HDL as shown in Fig. 7, and an HDL controller 300' that forms and outputs a signal for decoding the HDL statement and constructing the corresponding logical function using the self-construction circuit 100 are provided.

Hereupon, the HDL controller 300' that decodes the HDL statement has the same configuration as a CPU of a microprogram control system, for example, that is, it can construct a memory (micro ROM) that stores a microprogram in which the procedure for processing each HDL language is described, a control circuit that performs the read sequence control of the memory, and a decoder circuit that decodes the read microinstruction and forms a control signal. Since the HDL is massive and the syntax is also comparatively simple, it can sufficiently be constructed on a single semiconductor chip with the current semiconductor integrated circuit technique.

Besides, Fig. 14 shows that the memory circuit 10 of which the main unit is a memory array and the variable address conversion circuit 30 are arranged in a memory space. This means

that the memory array 11 that constructs the memory circuit 10 and the memory array 31 that constructs the variable address conversion circuit 30 may be also arranged in another area of the same memory array. The address decoders 12 and 32, comparator 14, data storage 60, and switch matrix 70 are collectively shown as an addressing circuit.

Since the data storage 60 described in the embodiment of Fig. 8 is a kind of a memory, it can be also arranged in another area in a memory array together with the memory array 11 that constructs the memory circuit 10 and the memory array 31 that constructs the variable address conversion circuit 30 in accordance with the same idea as described above. Further, an HDL storage that stores the design data described in the HDL ought to be also constructed so as to be arranged in another area of a single memory array together with the memory array 11 that constructs the memory circuit 10.

The invention produced by this inventor is specifically described above based on the embodiment. However, the present invention is not limited to the above embodiment, and, needless to say, can variously be modified within the range where its point will not be deviated. For example, a logic gate circuit to be constructed is not limited to a NAND gate, but may be also a NOR gate, an AND gate, and an OR gate. Further, a flip-flop circuit to be constructed is also limited to that having only two NAND gates as shown in Fig. 11, but may be also an RS flip-flop

having a reset terminal and a set terminal.

INDUSTRIAL APPLICABILITY

In the above description, the invention produced by this inventor is mainly described quoting a design technique of a logic integrated circuit that is a field of application as its background. However, the present invention is not limited to this design technique. For example, the present invention can also be used in the development of a semiconductor integrated circuit in which a logic circuit and an analog circuit are mixed on a single semiconductor chip.

CLAIMS:

1. A semiconductor integrated circuit, comprising:

storing means that enables reading and writing;

comparing means that compare write data supplied to the storing means with data read from the storing means; and

variable address converting means that convert an address signal supplied to the storing means based on a comparison result in the comparing means, wherein an input signal of a logic circuit having a desired logical function is input as the address signal to the storing means, and wherein the data is written to the storing means so that the read data of the storing means can be obtained as an expected output signal with respect to the input signal of the logic circuit.

2. A semiconductor integrated circuit according to claim 1, wherein a plurality of the storing means, a plurality of the comparing means, and a plurality of the variable address converting means are provided on a single semiconductor chip.

3. A semiconductor integrated circuit according to claim 1 or 2, wherein the storing means are a volatile memory.

4. A semiconductor integrated circuit according to claim 1, 2, or 3, wherein the variable address converting means comprise: a memory array in which a plurality of memory cells

are arranged in a matrix shape; an address decoder that selects the memory cells in the memory array based on an input address signal; reading means that amplify a signal read from the memory array; and operating means that update the input address signal based on a control signal.

5. A semiconductor integrated circuit according to claim 4, wherein the memory array has the volatile memory.

6. A semiconductor integrated circuit according to claim 1, 2, 3, 4, or 5, further comprising: data holding means that can hold the data read from the storing means; a switch matrix that switches the input address signal or an output signal of the data holding means and can supply it to the variable address converting means; and the storing means that store the control information of each switch in the switch matrix.

7. A semiconductor integrated circuit according to claim 6, wherein the data holding means comprise: latching means that can latch first data read from the memory circuit; and gate means that permit or do not permit latching of the first data to the latching means based on the first data read from the memory circuit.

8. A method for constructing a logic integrated circuit,

wherein the logic integrated circuit having a desired logical function is constructed by decoding design data of a function level described in HDL by control means using the semiconductor integrated circuit according to claim 1, 2, 3, 4, 5, 6, or 7 and assigning to the self-construction circuit a signal that decides a logical configuration of a self-construction circuit capable of constructing optional logic from the control means.

9. A method for constructing the logic integrated circuit according to claim 8, wherein the control means are formed on the same semiconductor chip as the self-construction circuit.

10. A method for constructing the logic integrated circuit according to claim 9, wherein a storage that stores the design data of the function level are formed on the same semiconductor chip as the control means and the self-construction circuit.

11. A semiconductor integrated circuit, comprising storing means that hold information obtained from a description in which a logical function is represented in hardware description language and obtain the output of the logical function that complies with an input signal from the output terminal, using the signal supplied to the address terminal as the input signal.

12. A semiconductor integrated circuit according to claim 11, wherein the logical function includes a combinational logical function.

13. A semiconductor integrated circuit according to claim 12, wherein the logical function includes a sequential logical function.

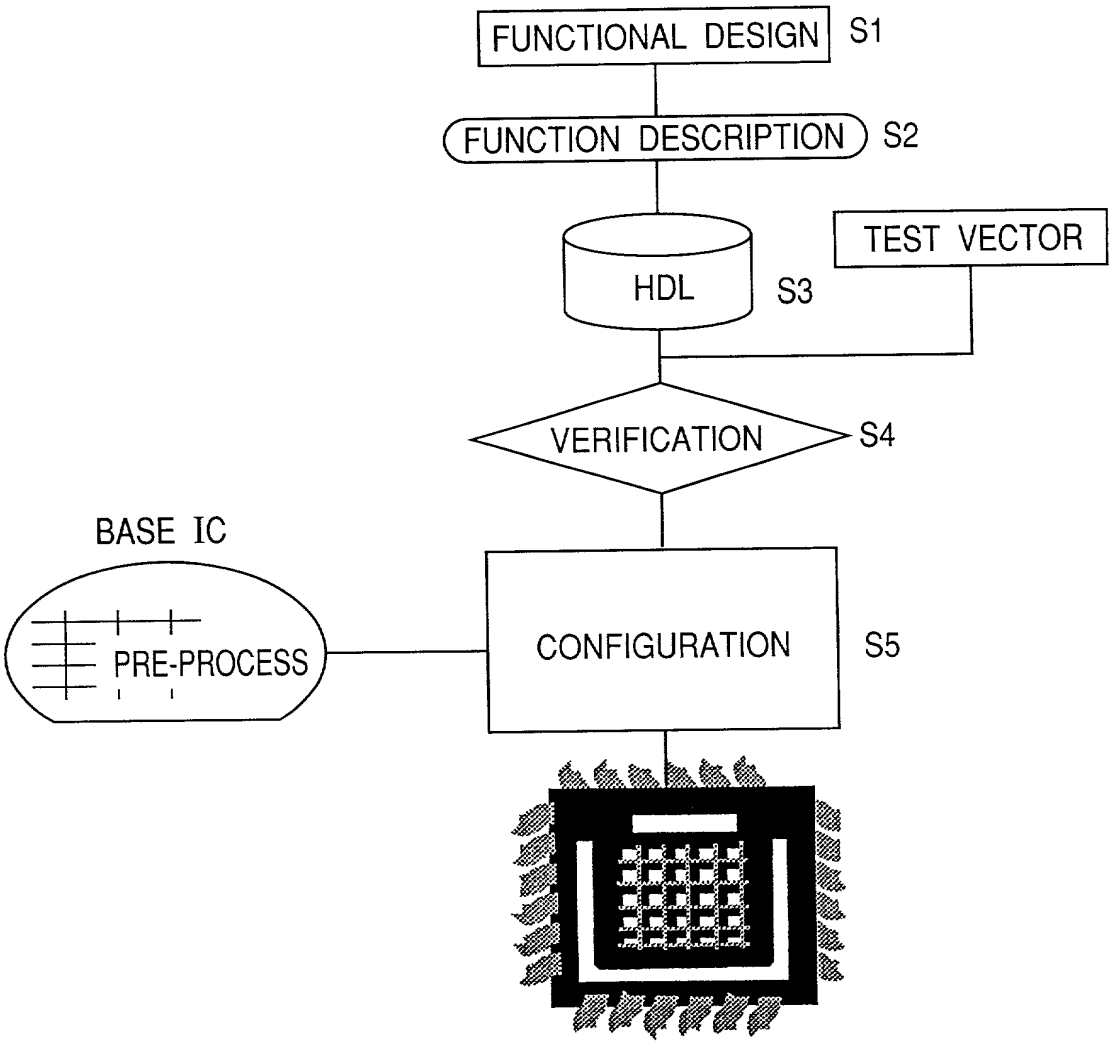
14. A semiconductor integrated circuit according to claim 11, wherein the storing means are read- and write-enable storing means.

15. A semiconductor integrated circuit according to claim 11, wherein converting means that form the information written to the storing means from the description represented in the hardware description language and the storing means are formed on the same semiconductor chip.

16. A semiconductor integrated circuit according to claim 15, wherein the storing means that hold the description represented in the hardware description language are formed on the semiconductor chip.

09/914429

FIG. 1



09/914429

FIG. 2

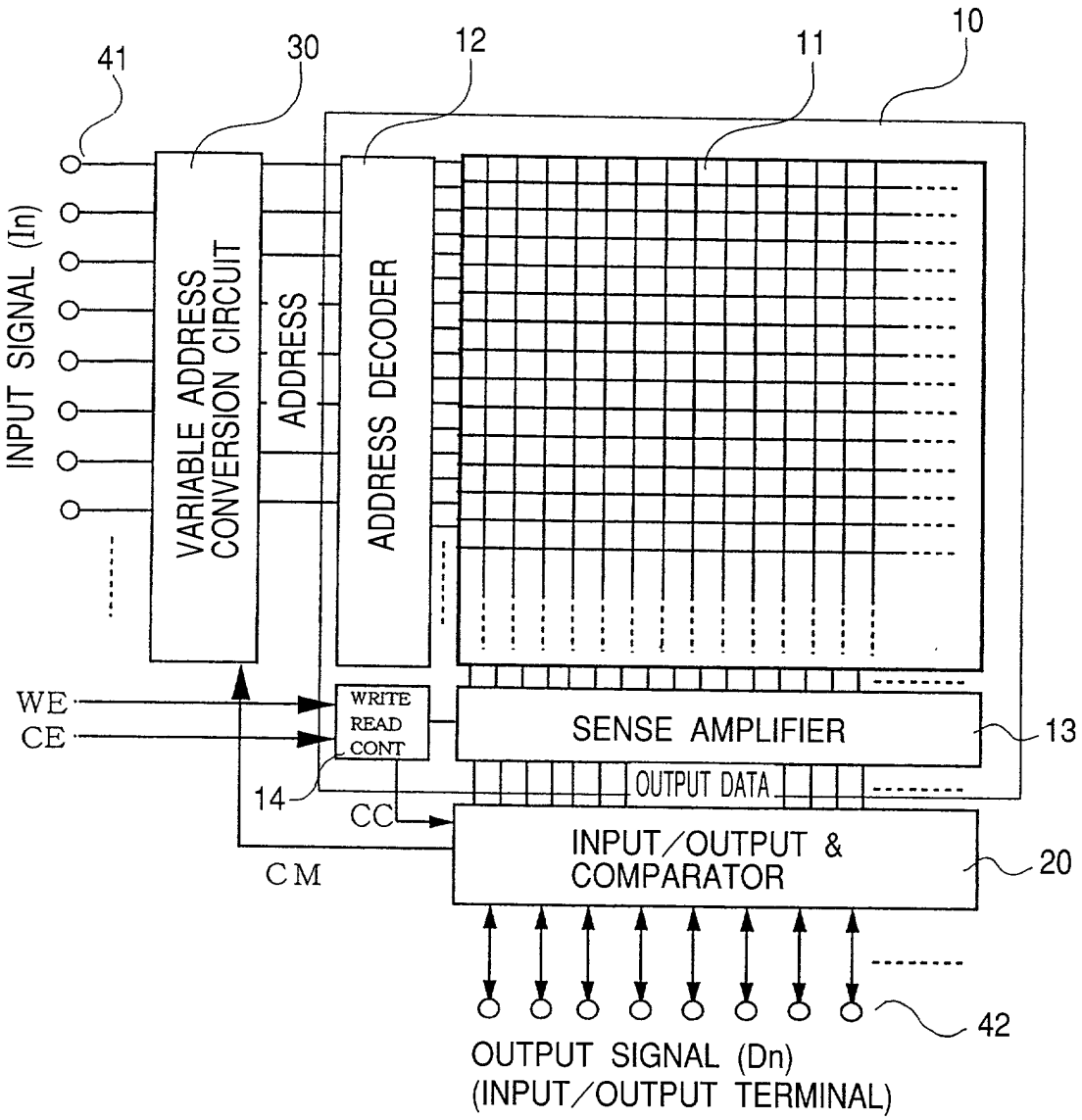


FIG. 3

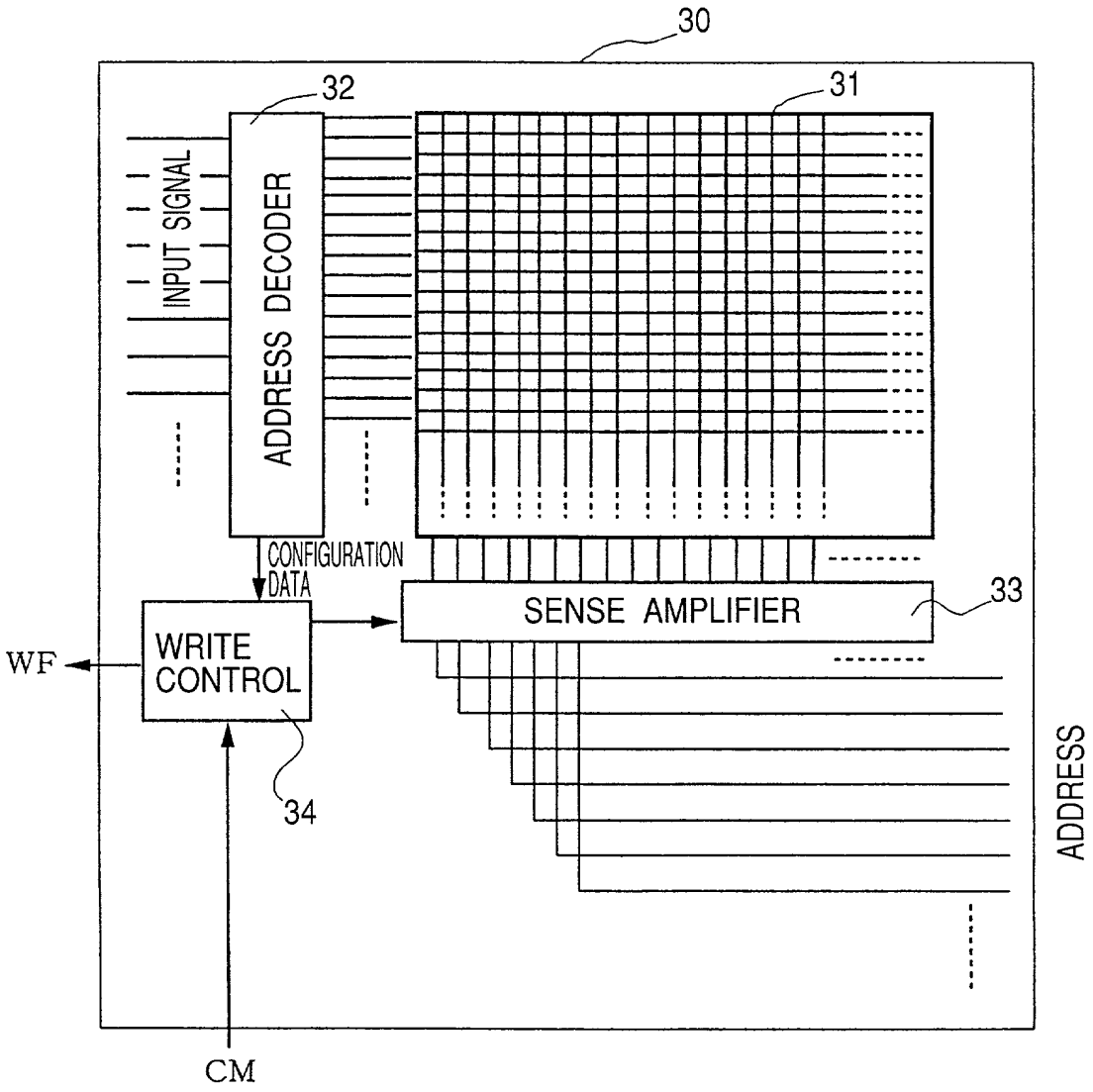


FIG. 4

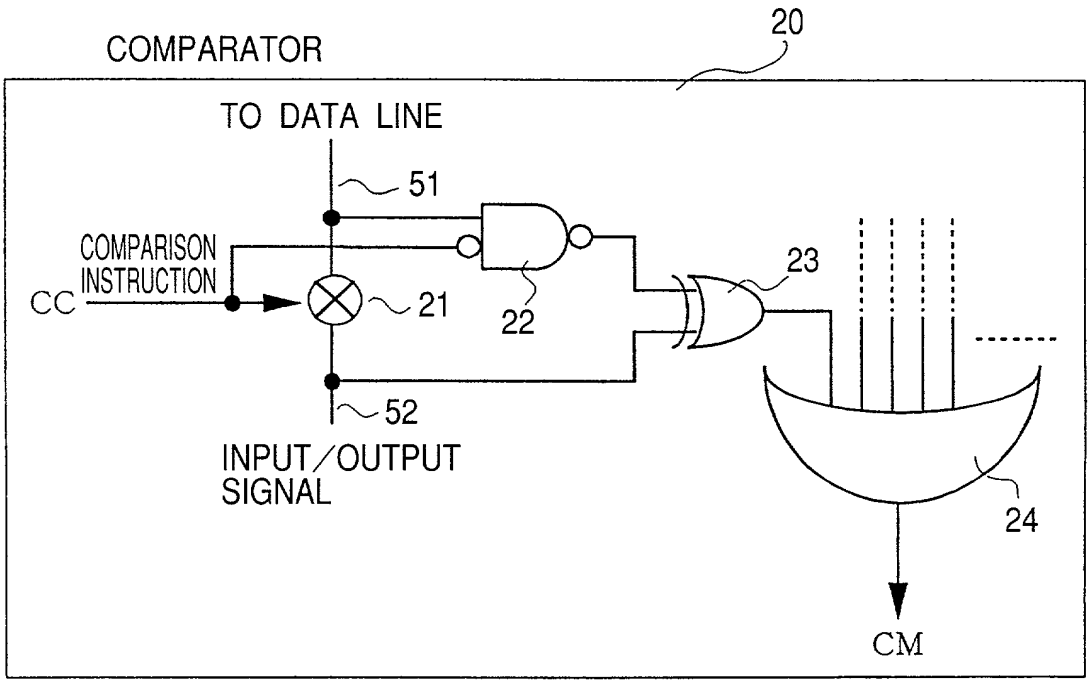

COMPARATOR
20
TO DATA LINE
51
COMPARISON INSTRUCTION
CC
21
22
23
52
INPUT/OUTPUT SIGNAL
24
CM

FIG. 5

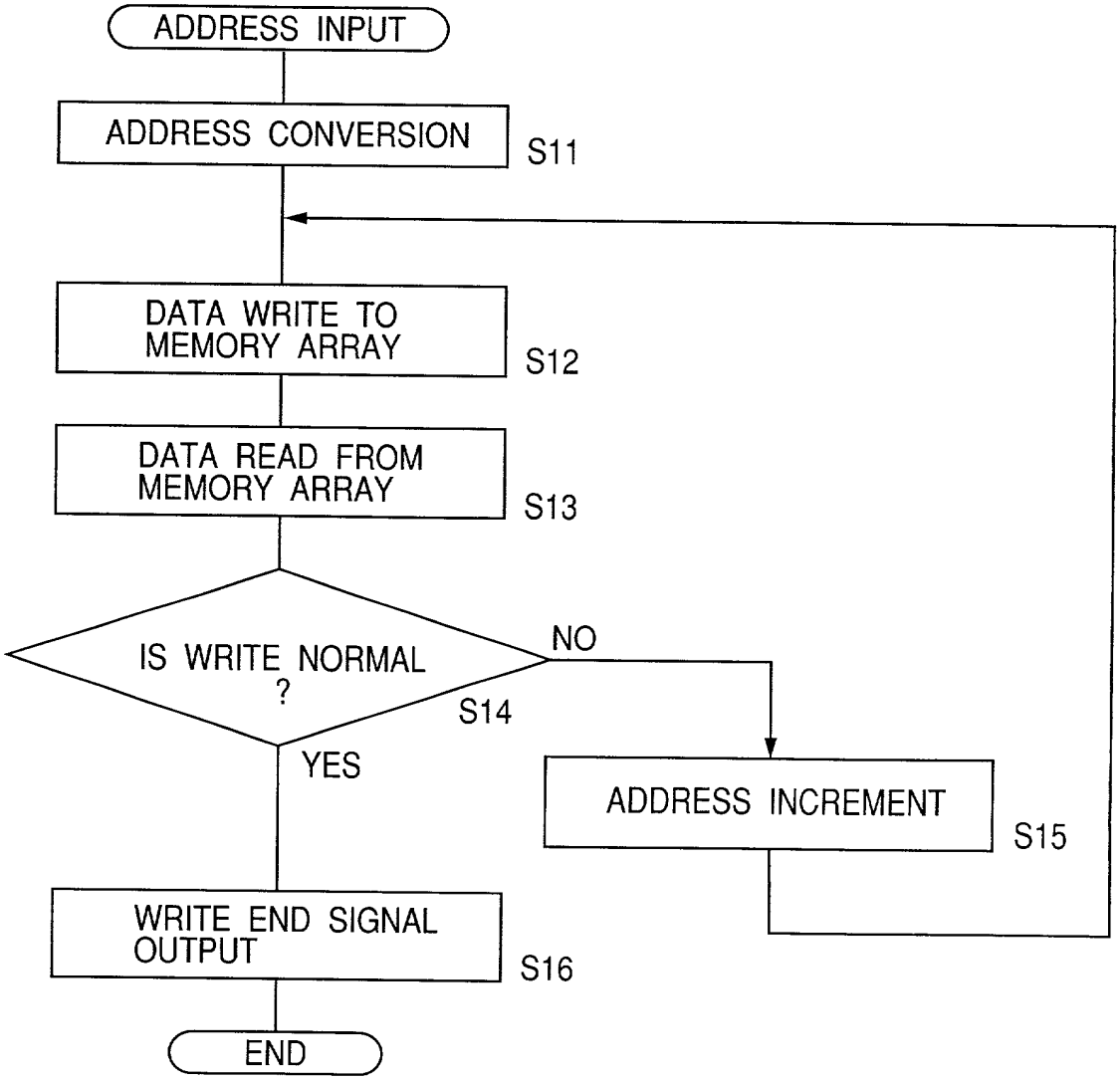
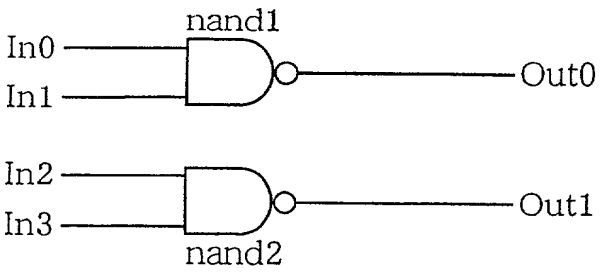

ADDRESS INPUT
ADDRESS CONVERSION
S11
DATA WRITE TO MEMORY ARRAY
S12
DATA READ FROM MEMORY ARRAY
S13
IS WRITE NORMAL ?
S14
NO
YES
ADDRESS INCREMENT
S15
WRITE END SIGNAL OUTPUT
S16
END

FIG. 6



HDL DESCRIPTIVE STATEMENT

```
//External Declaration
module nand1_gate(
 In0.
 In1.
 Out0
);
//Internal Declarations
input In0;
input In1;

wire In0;
wire In1;
reg Out0;
always @ (In0 or In1) begin

  //Block 1
  case(In0, In1)
   2'b 00:
      Out0=1'b1;
   2'b 01:
      Out0=1'b1;
   2'b 10:
      Out0=1'b1;
   2'b 11:
      Out0=1'b0;
   default
      ;
  endcase
end
endmododule // nand1_gate
//External Declaration
module nand2_gate(
 In2.
 In2.
 Out1);
//Internal Declarations
input In2;
input In3;

wire In2;
wire In3;
reg Out1;
always @ (In2 or In3) begin
  //Block 1
  case(In2, In3)
   2'b 00:
      Out1=1'b1;
   2'b 01:
      Out1=1'b1;
   2'b 10:
      Out1=1'b1;
   2'b 11:
      Out1=1'b0;
   default
      ;
  endcase
end
endmododule // nand1_gate2
```

FIG. 7

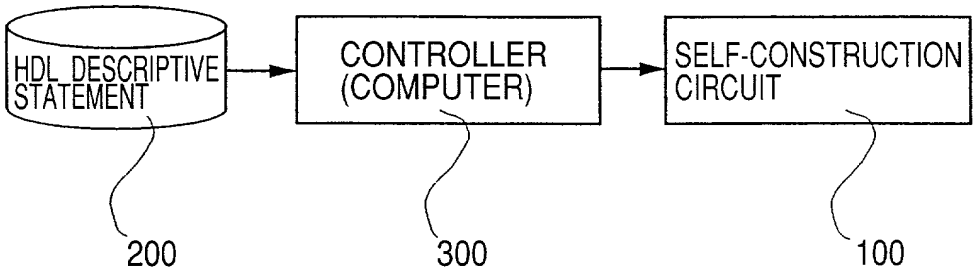


FIG. 8

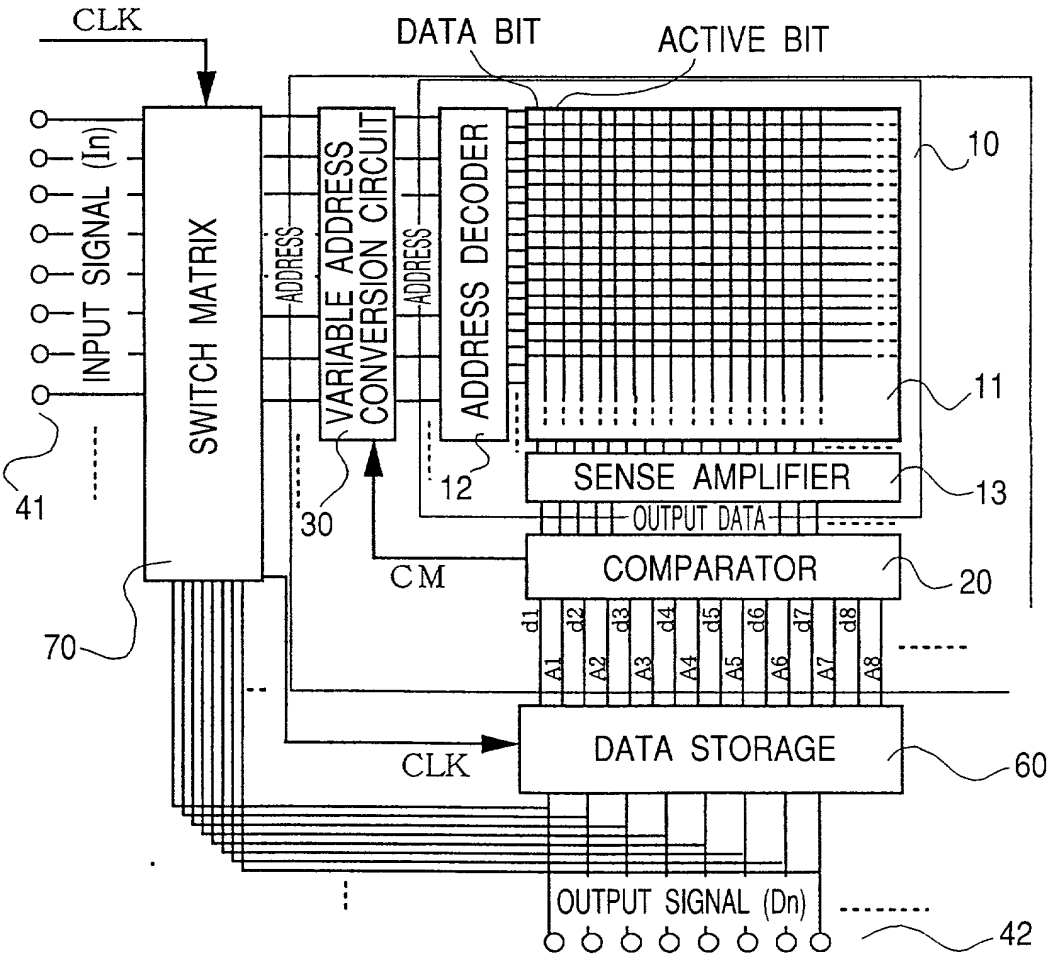


FIG. 9

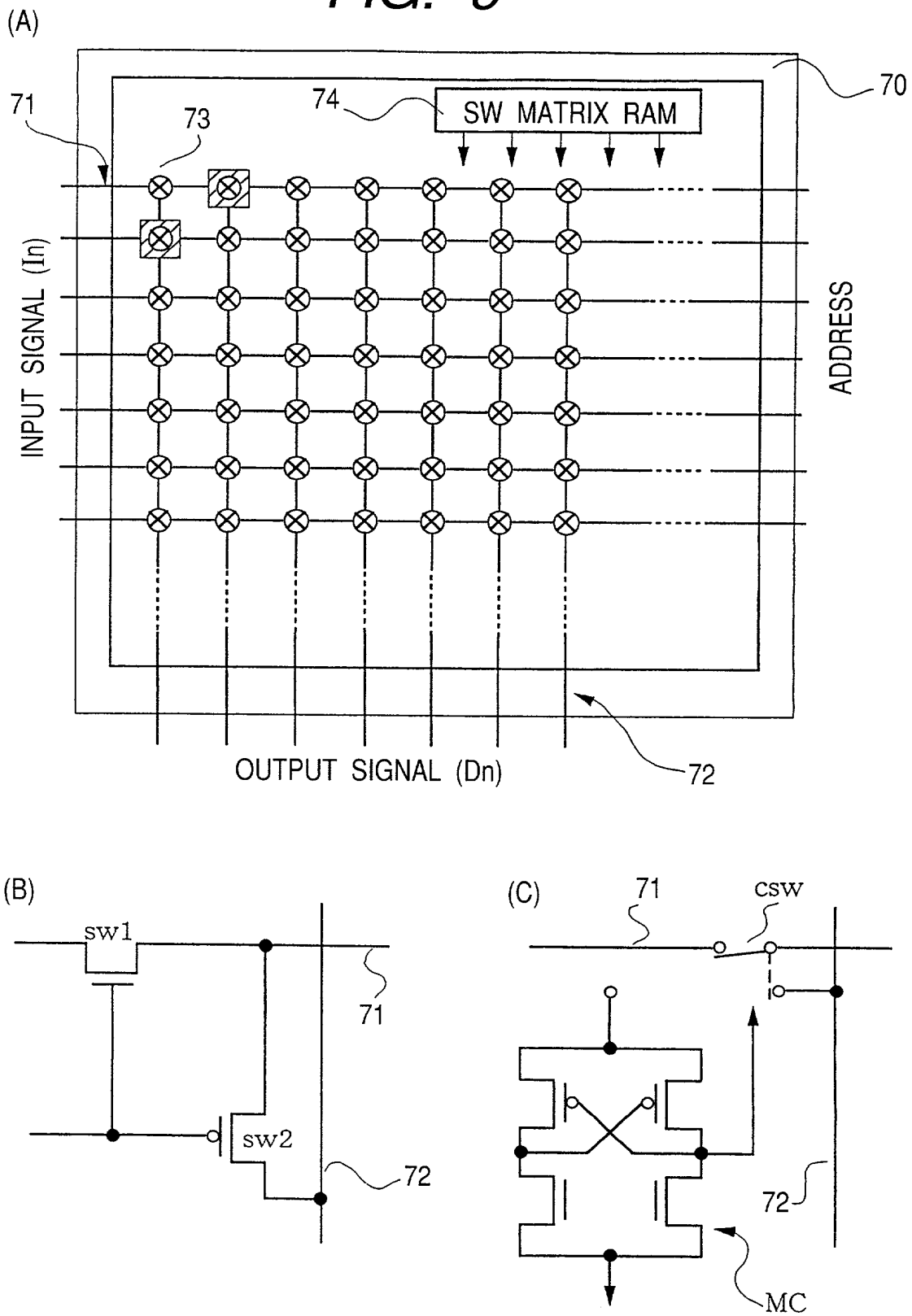


FIG. 10

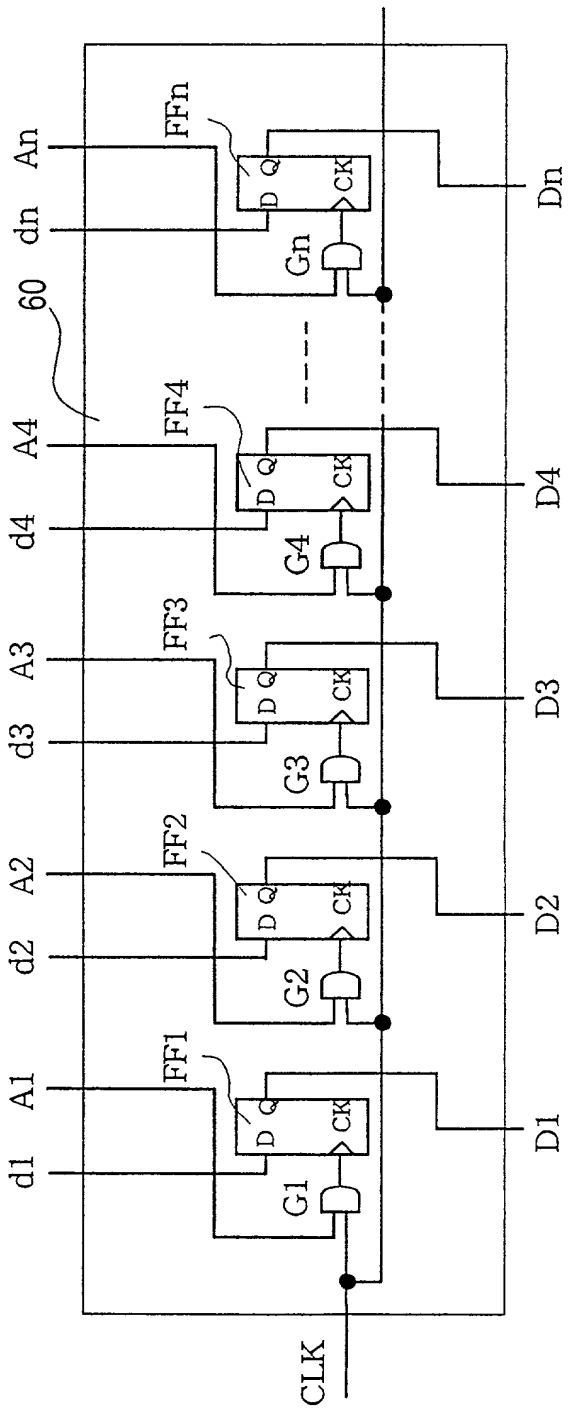
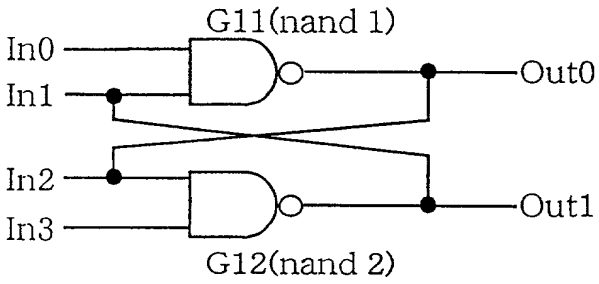

60
An
dn
FFn
Gn
Dn
A4
d4
FF4
G4
D4
A3
d3
FF3
G3
D3
A2
d2
FF2
G2
D2
A1
d1
FF1
G1
D1
CLK
D
Q
CK

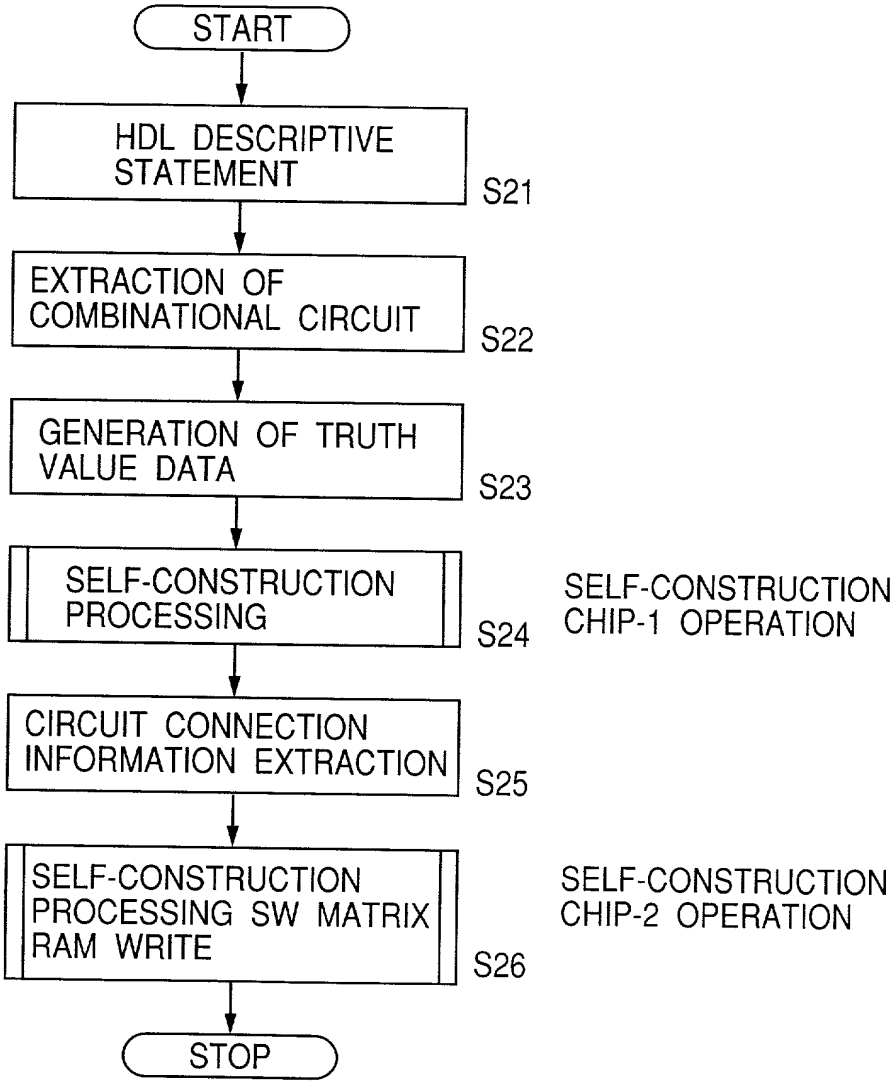
FIG. 11



HDL DESCRIPTIVE STATEMENT

```
//External Declaration
module ff model(
 In0,
 In1,
 Out0,
 Out1
);
//Internal Declarations
input In0;
input In1;
output Out0;
output Out1;
wire In0;
wire In1;
reg Out0;
reg Out1;
//Local declarations
//Instaces
nand1_gate(
 .In0 (In0),
 .In1 (Out1),
 .Out0 (Out0),
);
 nand2_gate(
 .In2 (Out0),
 .In3 (In3),
 .Out0 (Out1)
);
endmodule // ff_model
```

FIG. 12



09/914429

FIG. 13

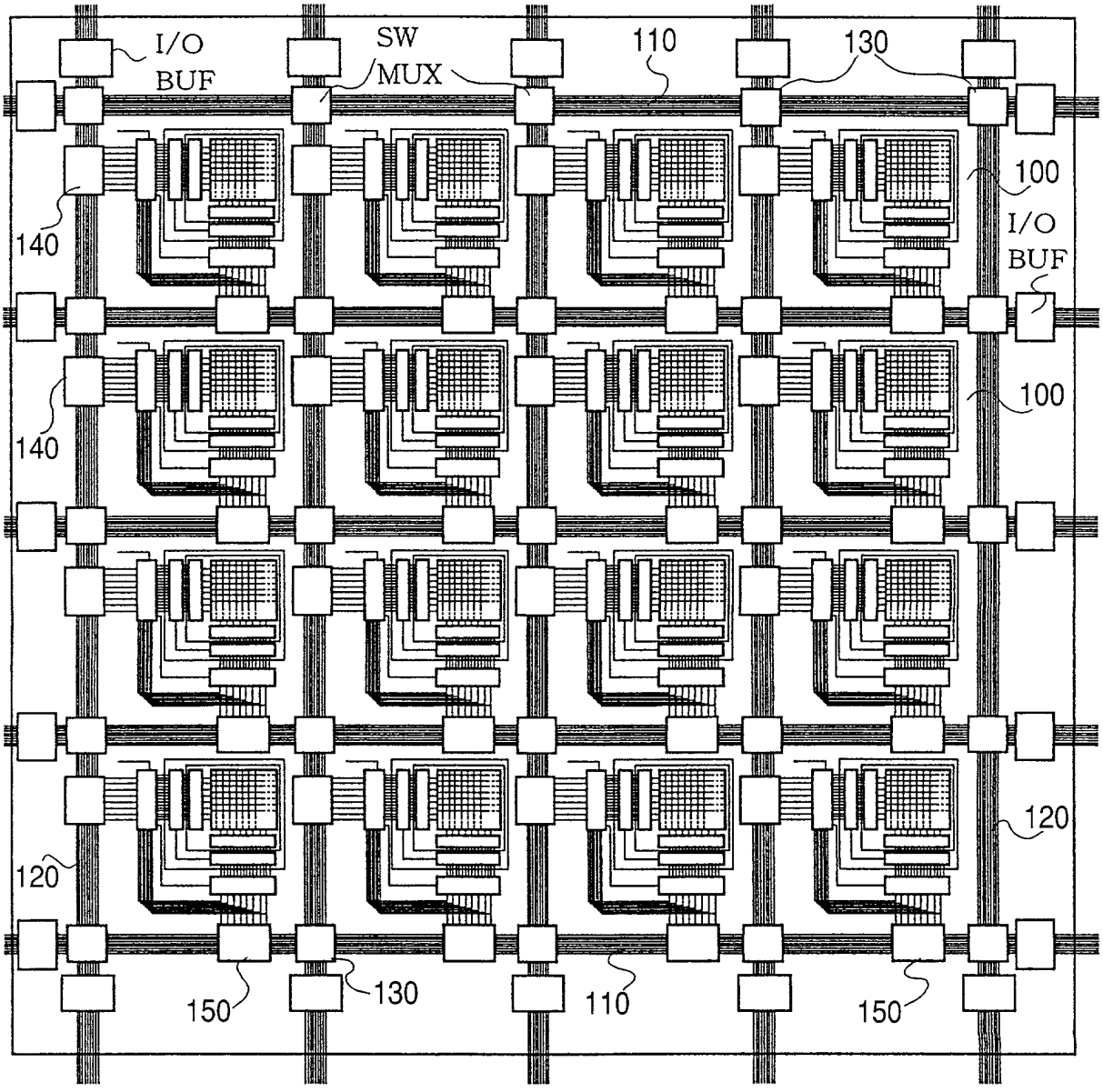


FIG. 14

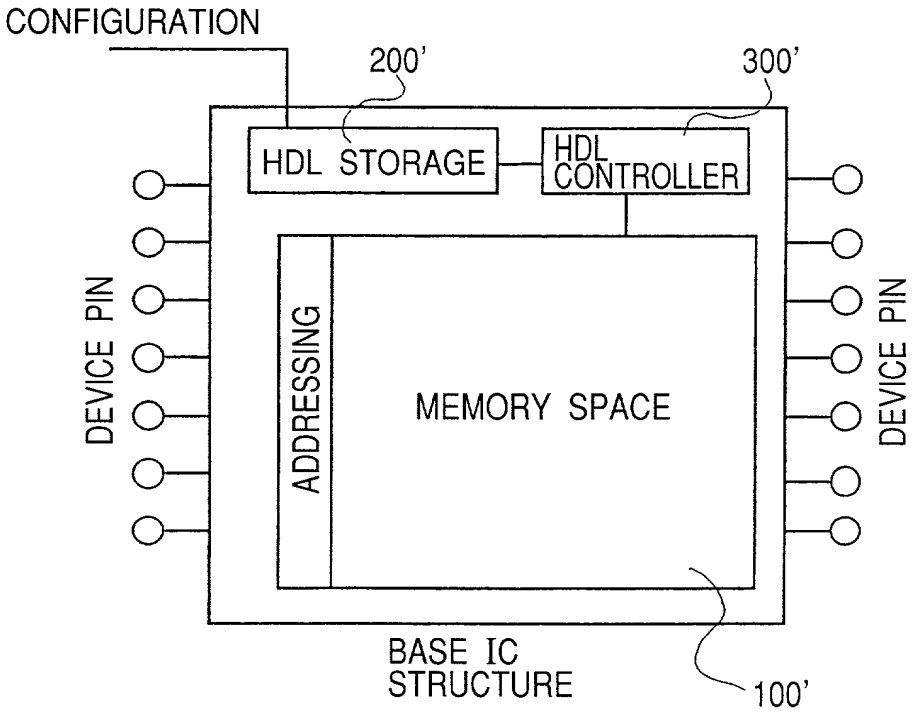
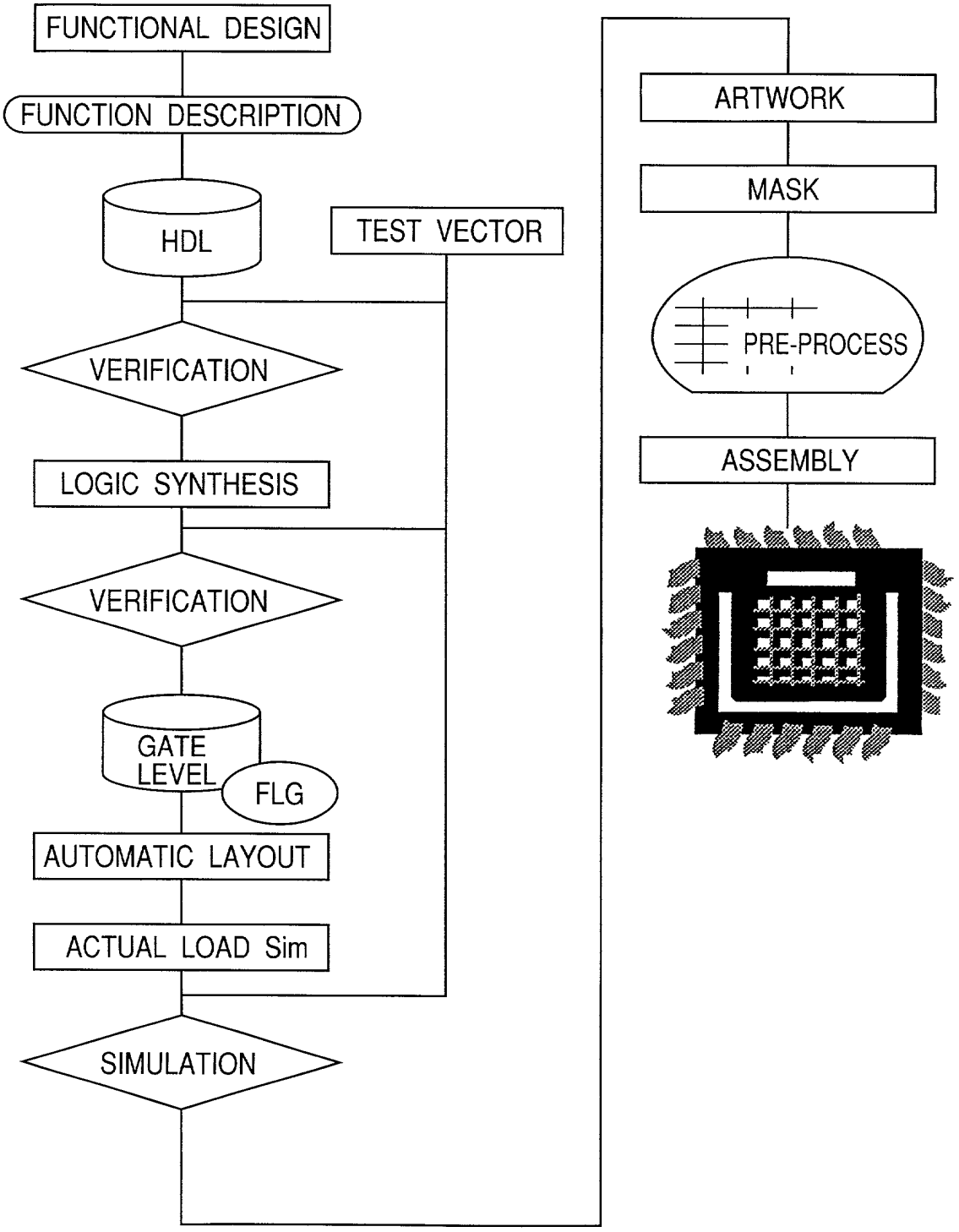

CONFIGURATION
200'
300'
HDL STORAGE
HDL CONTROLLER
ADDRESSING
MEMORY SPACE
DEVICE PIN
DEVICE PIN
BASE IC STRUCTURE
100'

FIG. 15


FUNCTIONAL DESIGN
FUNCTION DESCRIPTION
HDL
TEST VECTOR
VERIFICATION
LOGIC SYNTHESIS
VERIFICATION
GATE LEVEL
FLG
AUTOMATIC LAYOUT
ACTUAL LOAD Sim
SIMULATION
ARTWORK
MASK
PRE-PROCESS
ASSEMBLY

PTO/SB/106(8-96)
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Patent and Trademark Office; U.S. DEPARTMETNT OF COMMERCE

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD FOR DESIGNING LOGIC INTEGRATED CIRCUIT

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
(該当する場合) _____に訂正されました。

☐ was filed on 4/March/1999
as United States Application Number or
PCT International Application Number
PCT/JP99/01035 and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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Japanese Language Declaration
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私は、米国法典第３５編１１９条 (a) - (d) 項又は３６５条(b)項に基き下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約３６５ (a) 項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示している。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

Priority Not Claimed
優先権主張なし

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	☐

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I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条 (c) に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基ずいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基ずき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

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住所		Residence
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私書箱		Post Office Address

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(Supply similar information and signature for sixth and subsequent joint inventors.)

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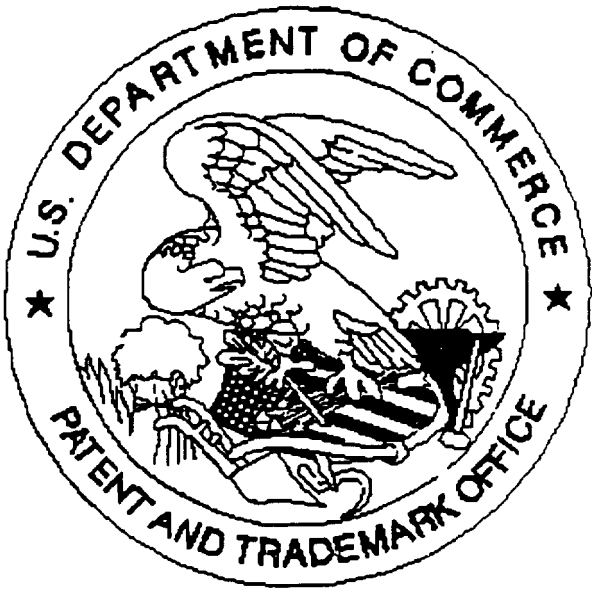

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